#9
Amdt A
J. Mk
4-5-02

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

YAMASAKI, KOZO, et al.

Appln. No.: 09/471,332

Confirmation No.: Unassigned

Group Art Unit: 2841

Filed: December 23, 1999

Examiner: Norris, J.

For: MULTILAYER-WIRING SUBSTRATE AND METHOD FOR FABRICATING SAME

AMENDMENT UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

Responsive to the outstanding Office Action of August 28, 2001, three times extended from November 28, 2001 to February 28, 2002 by the filing of an appropriate petition and payment for an extension of time submitted herewith, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 11 and 12 without prejudice or disclaimer.

Please enter the following amended claims:

A1

1. (Amended) A multilayer-wiring substrate comprising:

a first wiring conductor with a recessed surface formed by etching a surface of the first wiring conductor,

A1 Cont

a first insulating layer formed on a surface of the first wiring conductor except over the recess so that a first via-hole penetrates through the first insulating layer to the recessed surface; and

a second insulating layer formed on the other surface of the first wiring conductor, wherein a depth of the recess is 5-30 % of the thickness of the wiring conductor, and said conductor comprises copper.

A2

5. (Amended) A multilayer-wiring substrate comprising:

a first wiring conductor having top and bottom surfaces; a first insulating layer formed on the top surface of the first wiring conductor; a first via-hole penetrating through the first insulating layer; and a first columnar via-conductor formed in the via-hole,

wherein the first wiring conductor has a first recessed surface formed at the top surface of the first wiring conductor so that a bottom end of the first columnar via-conductor contacts the first recessed surface of the first wiring conductor, a depth of the recess is 5-30 % of the thickness of the wiring conductor, and said conductor comprises copper.

REMARKS

Claims 1 and 5 have been amended to incorporate therein the recitations of claims 11 and 12, to recite that the depth of the recess is 5-30% of the thickness of the wiring conductor and that the conductor comprises copper. Claims 11 and 12 have been canceled.

Entry of the amendments is respectfully requested.

Review and reconsideration on the merits are requested.

Claims 1, 2, 5 and 8 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,597,983 to Nguyen et al. Nguyen et al was cited as disclosing a first wiring conductor (20) having a recessed surface and a second conductor (30) contacting the first wiring conductor (20) through a via hole penetrating through a first insulating layer (24) over the recessed surface.

In response, claims 1 and 5 have been amended to incorporate therein the recitations of claims 11 and 12, to thereby obviate the rejection.

Claims 3, 4, 6, 7 and 9-12 were rejected under 35 U.S.C. § 102(a) as being unpatentable over Nguyen et al. The Examiner did not consider the limitations of the dependent claims to be of patentable significance.

Applicants traverse, and respectfully request the Examiner to reconsider in view of the amendment to claims and the following remarks.

The present invention seeks to correct the problem of residual resin accumulating at the bottoms of via holes formed by a photolithography method in a multilayer-wiring substrate, which residual resin hinders complete electrical contact between lower and upper conductors separated by an insulating layer. The invention has been achieved by providing a first wiring conductor with a recessed surface formed by etching a surface of the first wiring conductor, to

thereby remove resin fragments adhering to the conductor that forms a bottom of the via hole together with a portion of the conductor. That is, the bottom conductor is chemically etched using an etchant, which etches not only in the thickness direction but also in a planar direction of the bottom conductor. The chemical etching also undercuts the conductor underneath the residual resin fragments, thereby forming a recess in the bottom conductor as well as eliminating the fragments. Accordingly, the surface of the recessed area of the bottom conductor is cleaned up and the surface of the recessed conductor can be plated with a metal conductor, thereby assuring reliable electrical continuity and mechanical adhesion strength between upper and lower wiring conductors sandwiching the insulating layer (page 8, line 18 - page 9, line 9).

Nguyen et al is concerned with solving an entirely different problem encountered in the manufacture of integrated circuits on silicon wafers. In Nguyen et al, the insulating layers are silicon oxide layers and the conductors are made from aluminum (column 3, lines 1-6). A via 16 is opened through insulating 14 by anisotropic (RIE) etching through a masking layer (typically a photoresist masking layer). The resist masking layer is removed after the etching step (not shown by Nguyen et al). The RIE etching step deposits polymers 18 adhering to the sidewalls of the via 16. The prior art employed a mixture of hydrogen peroxide and sulfuric acid to remove the polymers 18, which attack the underlying conductive layer made from aluminum. This created undesirable holes in the aluminum (Fig. 2 and column 2, lines 39-51). Nguyen et al instead uses TMAH (a resist developer) remove the polymers without removing a substantial amount of aluminum (column 3, lines 11-28).

In order to more clearly distinguish the invention from the prior art, independent claims 1 and 5 have been amended to incorporate therein the recitation of claim 11, to recite that the depth of the recess is 5-30% of the thickness of the wiring conductor. Nguyen teaches away from purposely etching into the conductor in that Nguyen seeks to create vias and remove the sidewall polymer without removing a substantial amount of aluminum (column 30, lines 27-28).

Independent claims 1 and 5 have also been amended to recite that the conductor comprises copper, to thereby distinguish over the aluminum conductor of Nguyen. Particularly, Nguyen et al relates to integrated circuits having aluminum wiring, Nguyen et al seeks to preserve the aluminum wiring, and Nguyen et al teaches nothing about multilayer-wiring substrates comprising copper conductors.

Moreover, the problems solved by Nguyen et al (removing sidewall polymers deposited by RIE etching) and the present invention (removing accumulated resin at the bottom of the via hole) are entirely different, and the solutions proposed by Nguyen et al (using a resist developer which removes the sidewall polymers but does not substantially attack the aluminum wiring) and the present invention (using a chemical etchant for the specific purpose of partially etching the conductor and undercutting the accumulated resist) are entirely different, such that the invention is accordingly unobvious over Nguyen et al. Also any recess made in the aluminum wiring of Nguyen et al is undesirable, thereby teaching away from the present invention.

Regarding claim 4, Nguyen concerns an integrated circuit and does not have solder bumps. Regarding present claim 8 (the insulating layer comprises a material selected from resin, glass, ceramic, and mixtures thereof), the insulating layer of the invention is different from

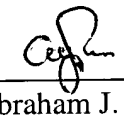
Nguyen et al which only speaks of silicon oxide insulating layers (see, for example, claim 4 of Nguyen et al).

In view of the above, it is submitted that the amended claims are patentable over the prior art, and withdrawal of the foregoing rejection is respectfully requested.

Withdrawal of all rejections and allowance of claims 1-10 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance the prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

Respectfully submitted,



Abraham J. Rosner
Registration No. 33,276

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: February 28, 2002